REMARKS

Claims 1-14 are pending in the present application. Reconsideration of the present application in view of the above amendments and the following remarks is respectfully requested. Claims 1 and 12 are amended herein to address matters of form and clarity only and not for reasons related to patentability. Thus claims 1 and 12 are entitled to the broadest possible scope of interpretation for the claim features recited therein including equivalents thereof.

Claims 6 and 9 have been rewritten in independent form only based on an indication of allowability of the original subject matter therein and have not otherwise been modified. Thus applicants believe that, notwithstanding the formality of amending the dependent claims to incorporate the features of the base claim thereinto, no amendments related to patentability are being performed and thus claims 6, 9, and their respective dependencies are entitled to the broadest possible scope of interpretation for the claim features recited therein including equivalents thereof.

Claims 1–3 and 12-14 stand rejected as being allegedly anticipated by Tamagawa, U.S. Patent No. 5,754,078. The rejection is respectfully traversed.

In making the rejection, the Examiner alleges that transistors Qp1, Qp2, Qn1, Qn2 described in Tamagawa amount to, for example, the claimed current control circuit of the present invention. A close review of Tamagawa, for example, at column 5, lines 36 to 43, reveals that the p-MOS transistors Qp1 and Qp2 constitute a current mirror, with Qp1 and Qp2 having the same transistor size. Specifically, the function of the p-MOS transistors Qp1 and Qp2 is to cause an equal current to flow through the resistors R1 and R2, respectively. Similarly, Tamagawa at column 5, lines 46-49, describes that the n-MOS transistors Qn1 and Qn2 constitute a current mirror, with Qn1 and Qn2 having the same transistor size. Specifically, the function of the n-MOS transistors Qn1 and Qp2 is to cause an equal current to flow through the resistors R3 and

R4, respectively. Tamagawa notably fails to disclose, for example, the claimed first and second transistors, and the current control unit *in the manner claimed* as required.

Accordingly, the p-MOS transistors Qp1, and Qp2 and the n-MOS transistors Qn1, and Qn2 of Tamagawa fail to perform the claimed functions associated with, for example, the control circuit of the present invention, namely detecting a current flowing in one of the first and second transistors, and causing a current to flow into the control terminal of the other of the first and second transistors and to make the other of the first and second transistors turn off.

In other words, based on the description in Tamagawa, transistors Qp1, Qp2 and Qn1, Qn2 are not configured to detect a current flowing in one of the first and second transistors, cause a current to flow into the control terminal of the other of the first and second transistors, and, make the other of the first and second transistors turn off.

It is submitted therefore that a *prima facie* case of anticipation has not been established in that Tamagawa fails to disclose all the claimed features as required. It is respectfully requested that the rejection of independent claims 1 and 12 be reconsidered and withdrawn.

Claims 2, 3, 13, and 14, by virtue of depending from claims 1 and 12 are allowable for at least the reasons set forth herein above with regard to claims 1 and 12. It is respectfully requested that the rejection of claims 2, 3, 13, and 14 be reconsidered and withdrawn.

Claims 1–5 and 12-14 stand rejected as being allegedly anticipated by Komatsu, et al., U.S. Patent No. 6,208,208B1 (hereinafter "Komatsu"). The rejection is respectfully traversed.

In making the rejection based on Komatsu, the Examiner alleges that transistors 104 and 204 in Komatsu amount the claimed first and second transistors, and the current mirror circuit 3, the current mirror circuit 4, the idling current setting circuit 2A, and the transistors 103, 203 in Komatsu amount to the claimed current control unit of the present invention.

A close review of Komatsu, for example at column 4, lines 16-25, reveals that the current mirror circuit 3 and the diode connection of the load transistor 103 allow the voltages at the inverted current inflow terminal 10 and the non-inverted current inflow terminal 11 to be maintained in almost the same and stable conditions. Similarly, for example as described in Komatsu at column 4, lines 26-35, the current mirror circuit 4 and the diode connection of the load transistor 203 allow the voltages at the inverted current inflow terminal 12 and the non-inverted current inflow terminal 13 to be maintained in almost the same and stable conditions.

Such conditions as described in Komatsu, cause negligible current flow between the non-inverted current terminal 11 and the constant-current inflow terminal 14, and similarly, cause negligible current flow between the inverted current terminal 12 and the constant-current inflow terminal 15. As further described in Komatsu, for example, at column 4, lines 36-46, the negligible current flow allows the idling current setting circuit 2 to optionally set an idling current, which flows through both the transistors 104 and 204.

Based on the foregoing analysis of the description in Komatsu, it is clear that notwithstanding the descriptions of the current mirror circuit 3, current mirror circuit 4, idling current setting circuit 2A, and transistors 103, 203, Komatsu fails to disclose claimed features including the claimed functions including detecting a current flowing in one of the first and second transistors, causing a current to flow into the control terminal of the other of the first and second transistors, and making the other of the first and second transistors turn off.

Accordingly, a *prima facie* case of anticipation has not been established in that Komatsu fails to disclose all the claimed features as required. It is respectfully requested that the rejection of independent claims 1 and 12 be reconsidered and withdrawn.

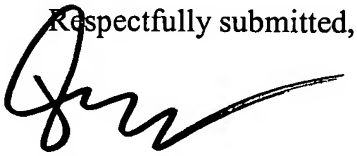
Claims 2,-5, 13, and 14, by virtue of depending from claims 1 and 12 are allowable for at least the reasons set forth herein above with regard to claims 1 and 12. It is respectfully requested that the rejection of claims 2,-5, 13, and 14 be reconsidered and withdrawn.

The indication of allowability with regard to claims 6-11 is noted with appreciation. Claims 6 and 9 are amended herein into independent form only including all of the limitations of the base claim and intervening claims. Thus, claims 6-11 should be placed in condition for allowance.

In view of the foregoing, the Applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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